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Abstract
This thesis is to design a 24-bit audio processor using automatic verilog code generation method. The processor is based on RISC architecture to get better performance for audio compression and decompression. Three algorithms: G.711(A-Law , u-Law)、ADPCM and MELP(Mixed Excitation Linear Prediction) will be implemented as examples of using proposed audio processor.

Using automatic Verilog RTL Code design can reduce the factitious mistakes and shorten design time. The design procedures are as follows. First is to define the instruction set、SFR、ALU、and addressing mode,…,etc. We demonstrate that only using 23 instructions one can achieve all the required algorithms described in the above. Then a C/C++ program is used to generate the Verilog Code automatically.
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